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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,596	04/30/2001	Cornelis Bernardus Aloysius Wouters	PHNL 000240	4795

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	17

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,596	WOUTERS, CORNELIS BERNARDUS ALOYSIUS	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9 and 11-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9 and 11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 15 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed limitations are not supported by the specification as originally filed. Page 7, lines 25 – 29 of the specification that Applicant points to for support does not describe "a first iteration" or "a second iteration" of any steps. The passage merely describes a part of the selection process, that correspond to the determining step claimed in the parent claim, for wear level swapping of a block that exceeded the erase threshold value. These claims are interpreted in light of the portion of the specification that Applicant pointed to for support.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 15 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 15 recites the limitation " a first

iteration" and "a second iteration" in lines 3 and 4, respectively. The claim does not define what an iteration cycle consists of. It is not clear what is being repeated or iterated in "a first iteration" and "a second iteration".

Claim 17 is rejected for including the deficiencies of its parent claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 3, 5 – 9, 11 – 13 and 15 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assar *et al.* (PCT Publication No. WO 95/10083, hereinafter "Assar").

6. With respect to claims 1, 7, 13 and 15 – 17, Assar discloses a method of data management on a storage medium (figure 6, Flash Memory Device), the storage medium comprising a variety of blocks in which data can be stored, a first block from said variety being selected to execute a mutation on, characterized by determining whether the wear level of the first block is acceptable for executing the mutation, and if so, executing the mutation on the first block, and otherwise choosing from said variety a second block with a lower wear level than the first block, and copying the data of the second block to the first block (page 16, lines 19 – 29),

wherein the blocks from said variety have an associated counter for counting the number of mutations in the block concerned (figure 10, 620).

However, Assar does not specifically disclose that the limit value is increased when a predetermined number which is at least the majority of the counters of the blocks from said variety exceed the limit value, said determining being based on said limit value and a value of the counter of the first block. On the other hand Assar discloses a functionally equivalent method where the limit value is effectively increased when a predetermined number which is at least the majority of the counters of the blocks from said variety reach a maximum value (page 16, lines 19 – 31) by resetting the counters (see also figure 7, step 238). The limit values in Applicant's and Assar's inventions are used for wear leveling which is a mechanism used to ensure that all blocks are written to or erased fairly evenly. In both inventions, when an erasure count reaches a certain threshold, the data content of the block is swapped with one that is less frequently erased and the block that reached the threshold is not erased until the next wear leveling cycle. When the majority of block erasure counters reach the threshold (i.e. wear level is fairly even), the threshold is lifted, or increased, relative to the counters, so that the blocks can be erased (or written to) again and the wear leveling cycle begins anew. In Applicant's invention, the threshold value is increased by increasing the limit value while retaining the counter values. Assar's invention increases this threshold by maintaining the limit value while resetting (or decreasing) the counter values.

The difference between Assar and the claims is the method of increasing the threshold value relative to the counter values to start a new wear leveling cycle. However, this particular method of increasing the limit value while retaining the counter values, as opposed to retaining the limit value while resetting the counter values, does not have a disclosed purpose nor is it disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter of design choice to use the method of increase the threshold value for new wear leveling cycle as opposed to resetting the counter values, since applicant has not disclosed that Applicant's method of increasing the threshold value relative to the counter values (or any other method of increasing the threshold value relative the counter values), overcomes a deficiency in the prior art or is for any stated purpose.

Because a flash cell device has a maximum life in terms of erase-write cycles, there's a need to keep track of the total number of erase cycles to be able to determine the remaining life of a device. One would be motivated to use the method of increasing the limit value while keeping the total counts intact to be able to keep accurate track of the total number of erase cycles on a per block basis for optimal use of all of the blocks. On the other hand, the method of keeping the limit value while resetting the counter has the advantage of having smaller counters using less number of bits and requiring simpler comparison operations. However, since the total erase count is reset, the system can easily keep track of the overall wear level by keeping track of the number of wear-level cycle operations, but the total counts for individual blocks are lost. There are different advantages and disadvantages for each of the methods. A flash memory system designer

would be motivated to choose one or the other depending on his/her preference and design criteria.

7. Claims 1 – 3, 5 – 9, 11 – 13, and 15 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assar in view of Bruce *et al.* (US Patent No. 6,000,006, hereinafter "Bruce").

With respect to claims 1, 7, 13, 15 – 17, Assar discloses a method of data management on a storage medium (figure 6, Flash Memory Device), the storage medium comprising a variety of blocks in which data can be stored, a first block from said variety of blocks being selected to execute a mutation on, characterized by determining whether the wear level of the first block is acceptable for executing the mutation, and if so, executing the mutation on the first block, and otherwise choosing from said variety a second block with a lower wear level than the first block, and copying the data of the second block to the first block (page 16, lines 19 – 29),

wherein the blocks from said variety have an associated counter for counting the number of mutations in the block concerned (figure 10, 620).

However, while Assar discloses a functionally equivalent method of increasing the limit value where the limit value is effectively increased when a predetermined number which is at least the majority of the counters of the blocks from said variety reach a maximum value (page 16, lines 19 – 31) by resetting the counters (see also figure 7, step 238), Assar does not specifically disclose that the limit value is increased when a

predetermined number which is at least the majority of the counters of the blocks from said variety exceed the limit value, said determining being based on said limit value and a value of the counter of the first block. On the other hand, Bruce specifically discloses a method of data management on a storage medium comprising a variety of blocks in which data can be store, where the limit value is increased when a predetermined number which is at least the majority of the counters of the blocks from the variety of blocks exceed the limit value (abstract, last 4 sentences, col. 9, lines 13 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Assar and Bruce before him at the time the invention was made, to use the threshold adjustment teachings of the flash memory storage system of Bruce, in the flash memory storage system of Assar, in order to minimize excess writes to flash memory while re-mapping address to pages of flash memory and be able to use a unified table for re-mapping, wear-leveling, and caching flash memories (Bruce, col. 2, lines 55 – 59).

It also would have been obvious to one of ordinary skill in the art, having the teachings of Assar and Bruce before him at the time the invention was made, to use the threshold adjustment teachings of the flash memory storage system of Bruce, in the flash memory storage system of Assar, in order to be able to determine the total number of erase/write cycles to a given block of flash memory (Bruce, col. 2, lines 31 – 33). This allows for a more efficient and exact wear-leveling scheme (Bruce col. 2, lines 54 – 55).

8. With respect to claims 2 and 8, the method is characterized in that when the value of the counter of the first block is smaller than the limit value, the value of the counter is increased and the mutation is executed, and otherwise a block of which the counter has a lower value than the counter of the first block is chosen as the second block (Assar, page 16, lines 20 – 25).

9. With respect to claims 3 and 9, the method is characterized in that the lower value is the lowest value of the values of the counters of the blocks from said variety (Assar, page 16, lines 22 – 25).

10. With respect to claims 5 and 12, the method is characterized in that the second block is erased after the data of the second block have been copied to the first block (this is inherent in flash memory store as the flash memory cells need to erased before new information can be written).

11. With respect to claim 6, the method is characterized in that the mutation comprises erasing the first block (Assar, page 16, lines 22 – 25).

12. With respect to claim 11, the system is characterized in that the system is arranged for initially constructing a table in which the value of the counters of the blocks are stated (Assar, figure 9).

13. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Assar, or Asser in view of Bruce as applied to claim 1 above, and further in view of Masters (US Patent No. 6,092,160).

Asser and Bruce disclose all of the limitations of the parent claim as discussed above. However, they do not specifically disclose that said copying is preceded by the step of copying to another block any stored data of said first block that is not marked for erasure. On the other hand, Bruce discloses swapping blocks for wear leveling (col. 7, lines 51 – 54). Masters discloses a method of wear-leveling flash memory where copying of less frequently used second block to the more frequently used first block involves swapping the data between the first block and the second block (Masters, figure 5, 512).

Applicants claimed step is a specific sequence in the swapping operation where the content of the first block is temporarily stored in a third location before the content of the second block is copied to the first block, so that the original data in the first block is preserved and copied over to the second block to complete the swapping operation. The use of a third storage location is inherent in a data swapping operation, as a temporary storage location is required to be able to swap data without losing any information. As to the specific sequence of steps in a swapping operation, one skilled in the art would recognize that there are two ways to perform the swapping operation, just as there are two ways to add two numbers to obtains a sum of two numbers. The first sequence is to copy the first block to a temporary store, copy the second block to the first block, and then copy the original content of the first block from the temporary store to the second block.

The second way is to copy the second block to the temporary store, copy the first block to the second block and finally copy the data from the second block from the temporary store to the first block. One skilled in the art would have further recognized that either sequence can be used equally effectively to swap the data, just as adding a first number to a second number is as effective as adding the second number to the first number in obtaining a sum of two numbers.

It also would have been obvious to one of ordinary skill in the art, having the teachings of Assar and Bruce before him at the time the invention was made, to use the data swapping for wear leveling teaching of the flash memory storage system of Masters, in the flash memory storage system of Assar, so that the little worn block becomes heavily used and wear on the heavily worn block is substantially reduced (Masters col. 9, lines 52 - 53).

Response to Amendment

14. Claim 15 has been amended to overcome an objection. Corresponding prior objection is withdrawn. However, the amendment did not address the rejection under 35 U.S.C. 112, second paragraph. This rejection is maintained in this action.

Response to Arguments

15. Applicant's arguments filed April 08, 2003 have been fully considered but they are not persuasive.

16. With respect to the rejection of claim 1, Applicant alleges lack of motivation citing one particular criterion (increased field size) among many that one skilled in the art would consider. However, Applicant offers reasons why Applicant would not be motivated but fails to address the motivation that was clearly cited, in the rejection of the claim in the last office action, in its entirety. The discussion of the motivation can be found on page 6 of the Office Action mailed October 10, 2003. The same motivation discussion is repeated in this action and will be repeated here again for convenience.

Because a flash cell device has a maximum life in terms of erase-write cycles, there's a need to keep track of the total number of erase cycles to be able to determine the remaining life of a device. One would be motivated to use the method of increasing the limit value while keeping the total counts intact to be able to keep accurate track of the total number of erase cycles on a per block basis for optimal use of all of the blocks. On the other hand, the method of keeping the limit value while resetting the counter has the advantage of having smaller counters using less number of bits and requiring simpler comparison operations. However, since the total erase count is reset, the system can easily keep track of the overall wear level by keeping track of the number of wear-level cycle operations, but the total counts for individual blocks are lost. There are different advantages and disadvantages for each of the methods. A flash memory system designer would be motivated to choose one or the other depending on his/her preference and design criteria.

17. Regarding Applicant's argument that alleges lack of motivation to combine Assar's and Bruce's teachings, again, Applicant fails to address the motivation cited in the rejection. Instead, Applicant cites sections of Bruce's prior art wear-leveling technique discussion for comparison with Assar's wear-leveling technique and concludes that because they are not the same there's no motivation to combine. Applicant suggests that because "Assar does not clear the erase counter until all blocks have the identical amount of usage (page 20, line 36 to page 21, line 2)" (page 9, lines 13 – 15, paper number 16) there's no motivation to redesign Assar in view of Bruce. The Examiner disagrees with Applicant's conclusion.

Two separate and independent motivations are cited in the rejection. The first motivation is to use the unified re-map, cache-index and wear-leveling counter table teaching of Bruce of which dual wear-leveling counter with increasing threshold is a major feature as evidence by the claims. Expressly stated desirability of this unified structure has not been address by Applicant. As for the second motivation, Bruce's motivation is to allows for a more efficient and exact wear-leveling scheme (Bruce col. 2, lines 54 – 55). Assar's wear-leveling scheme bases on periodic erasure of write counters may be better than the prior art system described by Bruce, it does not provide for "a more efficient and exact" wear-leveling scheme that Bruce's scheme does because the exact total erasure count is not kept. While Assar's "algorithm prevents any one portion of the memory storage from being erased a significant number of times more that any other portion" (Asser, page 21, lines 8 – 10), it does not allow for "a more efficient and

exact" wear-leveling scheme as Bruce desires because it does not keep track of exact total count.

18. As to Applicant's contention that Bruce fails to disclose or suggest, "increasing a limit value when a predetermined number... exceed the limit value", Applicant incorrectly states that "Bruce increases a limit value after a plurality of numbers exceed respective thresholds" (page 10, lines 1 – 5, amendment dated 4/8/04, paper number 16). Limit value is increased when most blocks reach or exceed the threshold (Bruce, col. 9, lines 9 – 20). According to Applicant's own argument, the majority (one of Webster's dictionary definition of most) is a predetermined number (see page 6, lines10 – 12, Amendment dated 9/16/03, paper number 12). Additionally, Asser teaches the functionally equivalent threshold adjustment when a predetermined number reach a threshold value as discussed in the rejection above. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

whc
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June 24, 2004

MATTHEW KIM
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